CBCS SCHEME

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15NT34

Third Semester B.E. Degree Examination, Feb./Mar. 2022
MOSFETs and Digital Circuits

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define JFET. Discuss the characteristics of JFET. **(08 Marks)**

b. Discuss the construction and characteristics of depletion of JFET. **(08 Marks)**

OR

2 a. With neat diagrams, explain n-well MOS Transistor Fabrication process. **(10 Marks)**

b. Write a short note on Second order effects in MOS. **(06 Marks)**

Module-2

3 a. Explain the Power dissipation equation for CMOS. **(06 Marks)**

b. Discuss the CMOS Transmission gates and Multiplexer. **(10 Marks)**

OR

4 a. Draw and explain Realization of CMOS NOR gate and NAND gate. **(10 Marks)**

b. Draw and explain the CMOS Inverter Voltage Transfer characteristics. **(06 Marks)**

Module-3

5 a. Realize the expression $Q^+ = CIK\ D + \overline{CIK}\ Q$ using CMOS transmission gate. **(06 Marks)**

b. Discuss Second order effects in MOS transistors. **(04 Marks)**

c. Discuss the working principle of Ring Oscillator. It is required to generate two clock signals that are complementary to each other. How can the Ring Oscillator used for this purpose? Can the Ring Oscillator be also used to generate clock signal with phase delays. Draw neat sketches to discuss. **(06 Marks)**

OR

6 a. It is required to drive a digital circuit using both positive level and negative level latch. Construct the positive and negative level sensitive latch using 2:1 multiplexers and CMOS inverters. Draw the CMOS circuit and discuss the working principle using timing diagrams. **(08 Marks)**

b. Define Setup time, Hold time and Clock to q delay using appropriate timing diagrams. **(04 Marks)**

c. Draw the CMOS circuit for 2 input XOR gate. **(04 Marks)**

Module-4

7 a. Define Registers. Explain PISO and SIPO shift registers **(08 Marks)**

b. Write a note on Johnson counter. **(04 Marks)**

c. Write a note on Ring counter. **(04 Marks)**

OR

8 a. Explain Modulus-8 synchronous up/down counter with a neat diagram. **(06 Marks)**

b. Using JK flip flop, design synchronous counter with the sequence 1, 3, 5, 2, 0, 7. **(10 Marks)**

Module-5

9 a. Explain Mealy and Moore machine models. **(08 Marks)**

b. Design a Mealy state diagram for the sequence 1101. **(08 Marks)**

OR

10 a. Design a Mod-8 synchronous counter using JK flip flop to count number of occurance of an input, i.e. No. of times it is 1. **(12 Marks)**

b. Construct a state table for the following state diagram. **(04 Marks)**

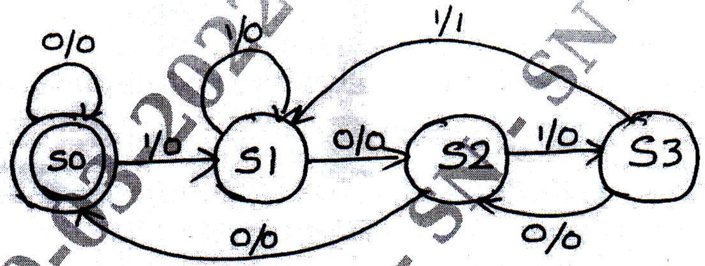

Fig.Q10 (b)

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